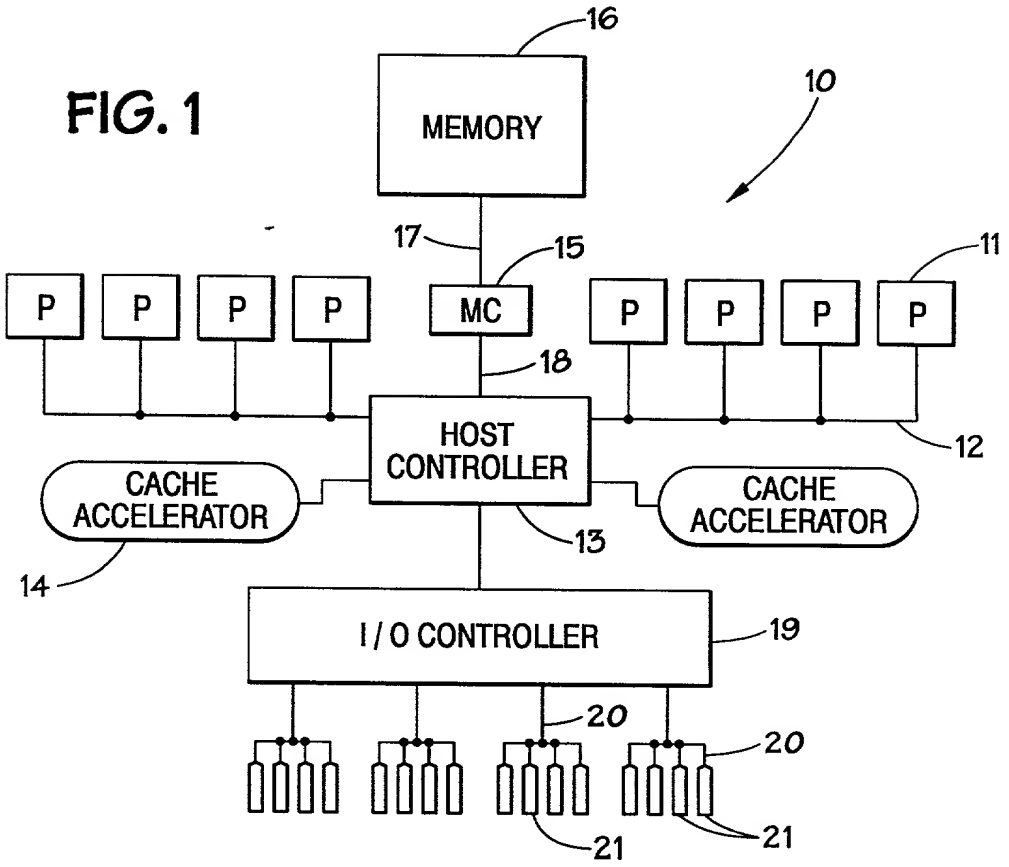
FIG. 1


16
MEMORY
10
17
15
11
P
P
P
P
MC
P
P
P
P
18
HOST CONTROLLER
12
CACHE ACCELERATOR
CACHE ACCELERATOR
13
14
I / O CONTROLLER
19
20
20
21
21

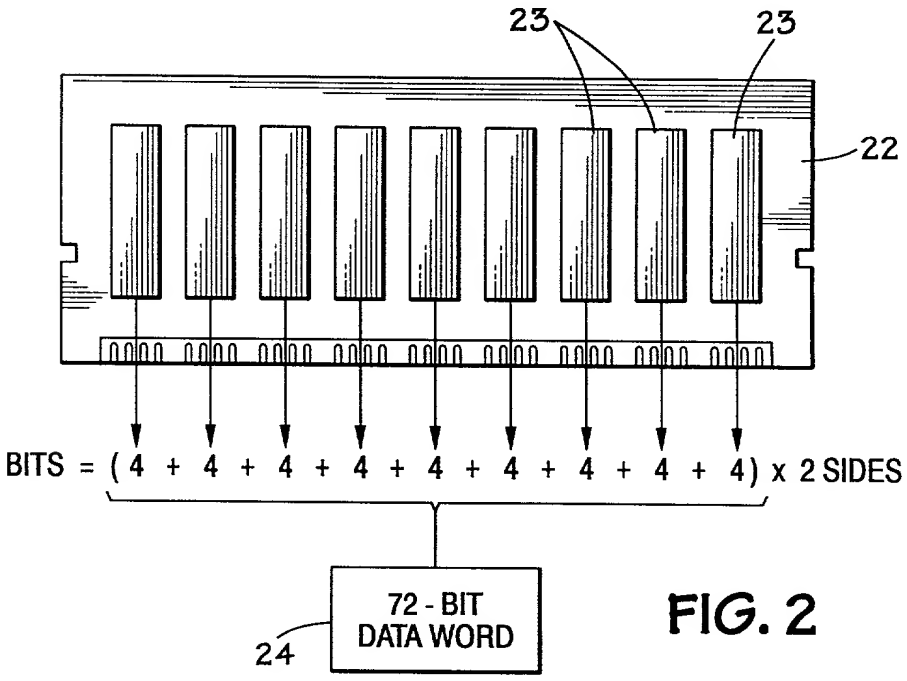

23
23
22
BITS = (4 + 4 + 4 + 4 + 4 + 4 + 4 + 4 + 4) x 2 SIDES
72 - BIT DATA WORD
24

FIG. 2

EXHIBIT 2003

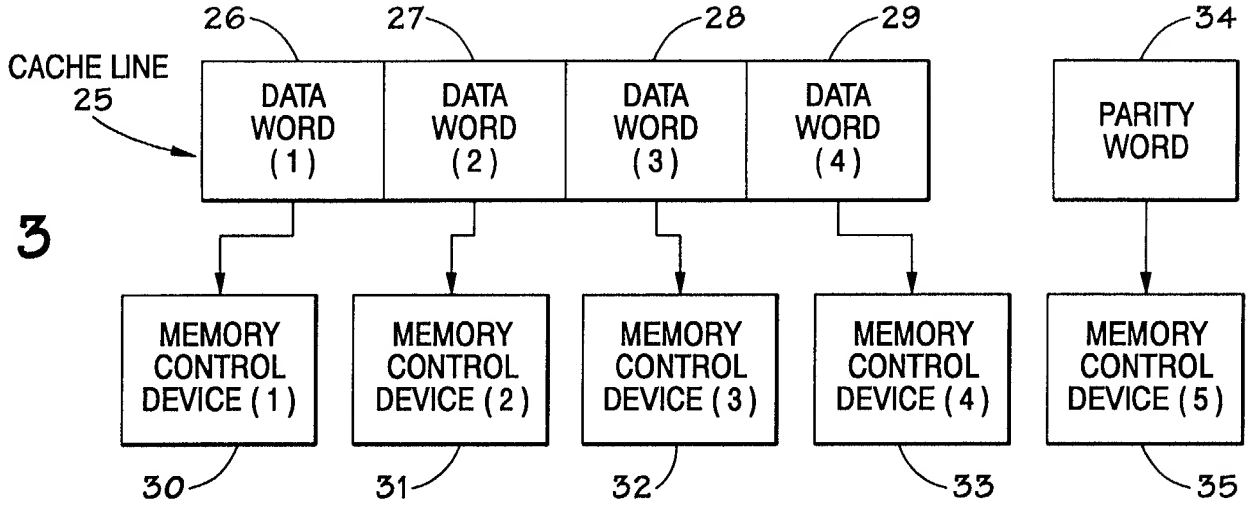


FIG. 3

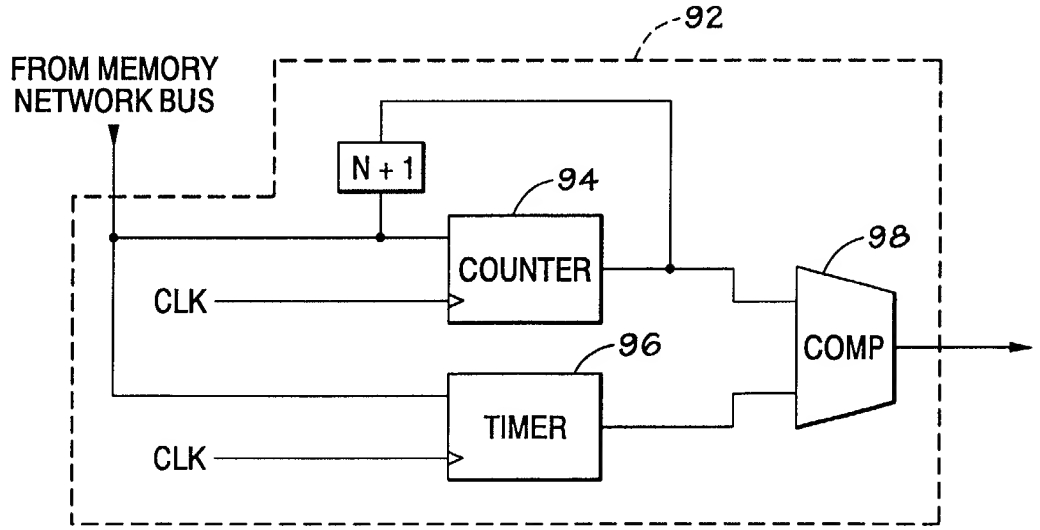


FIG. 8

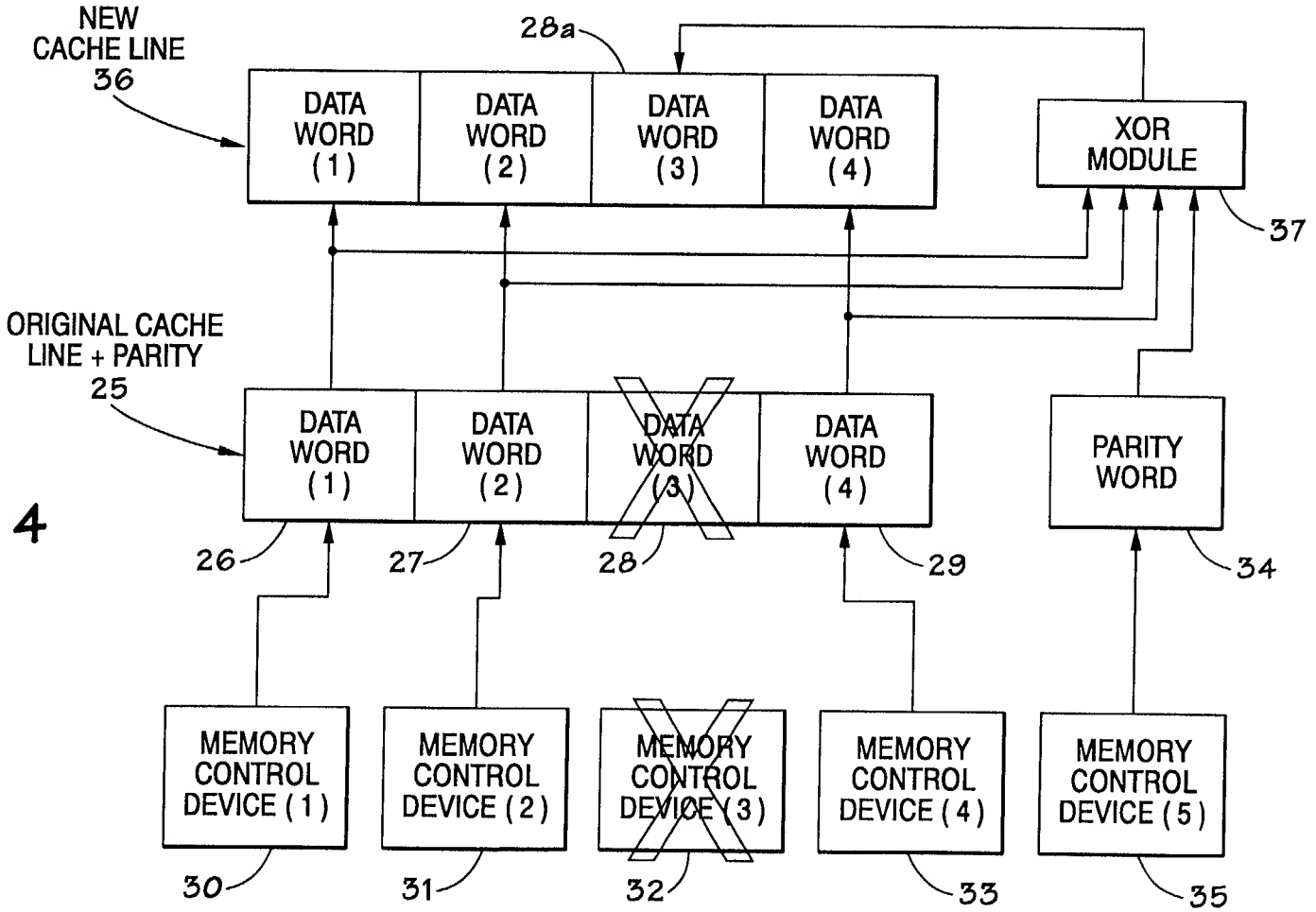

NEW CACHE LINE
36
28a
DATA WORD (1)
DATA WORD (2)
DATA WORD (3)
DATA WORD (4)
XOR MODULE
37
ORIGINAL CACHE LINE + PARITY
25
DATA WORD (1)
DATA WORD (2)
DATA WORD (3)
DATA WORD (4)
PARITY WORD
26
27
28
29
34
MEMORY CONTROL DEVICE (1)
MEMORY CONTROL DEVICE (2)
MEMORY CONTROL DEVICE (3)
MEMORY CONTROL DEVICE (4)
MEMORY CONTROL DEVICE (5)
30
31
32
33
35

FIG. 4

EP 0 926 926 A2

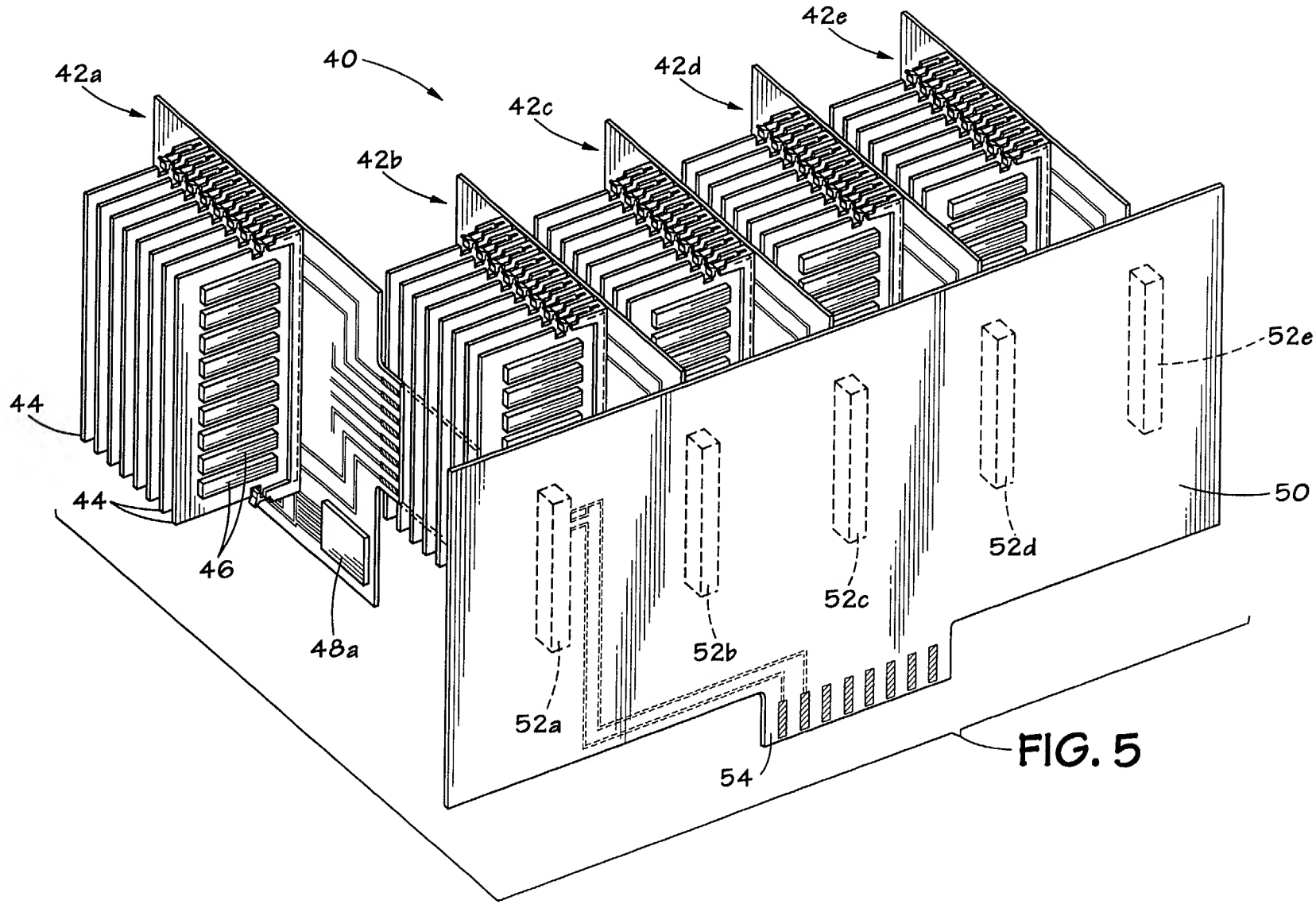
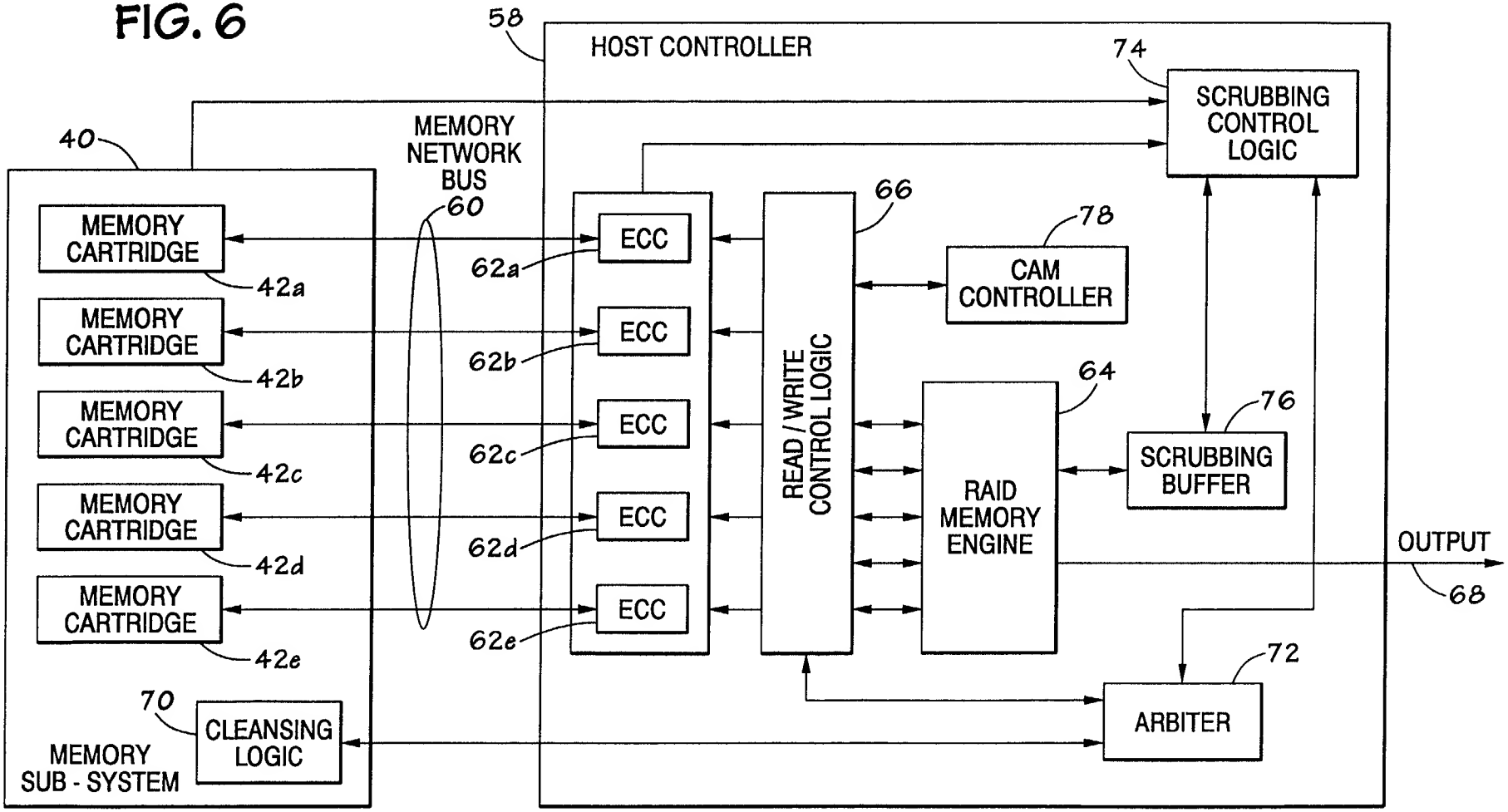


FIG. 5

FIG. 6


58
HOST CONTROLLER
74
SCRUBBING CONTROL LOGIC
40
MEMORY NETWORK BUS
60
MEMORY CARTRIDGE
42a
MEMORY CARTRIDGE
42b
MEMORY CARTRIDGE
42c
MEMORY CARTRIDGE
42d
MEMORY CARTRIDGE
42e
62a
62b
62c
62d
62e
ECC
ECC
ECC
ECC
ECC
66
READ / WRITE CONTROL LOGIC
78
CAM CONTROLLER
64
RAID MEMORY ENGINE
76
SCRUBBING BUFFER
OUTPUT
68
72
ARBITER
70
CLEANSING LOGIC
MEMORY SUB - SYSTEM

Tandem 92003200

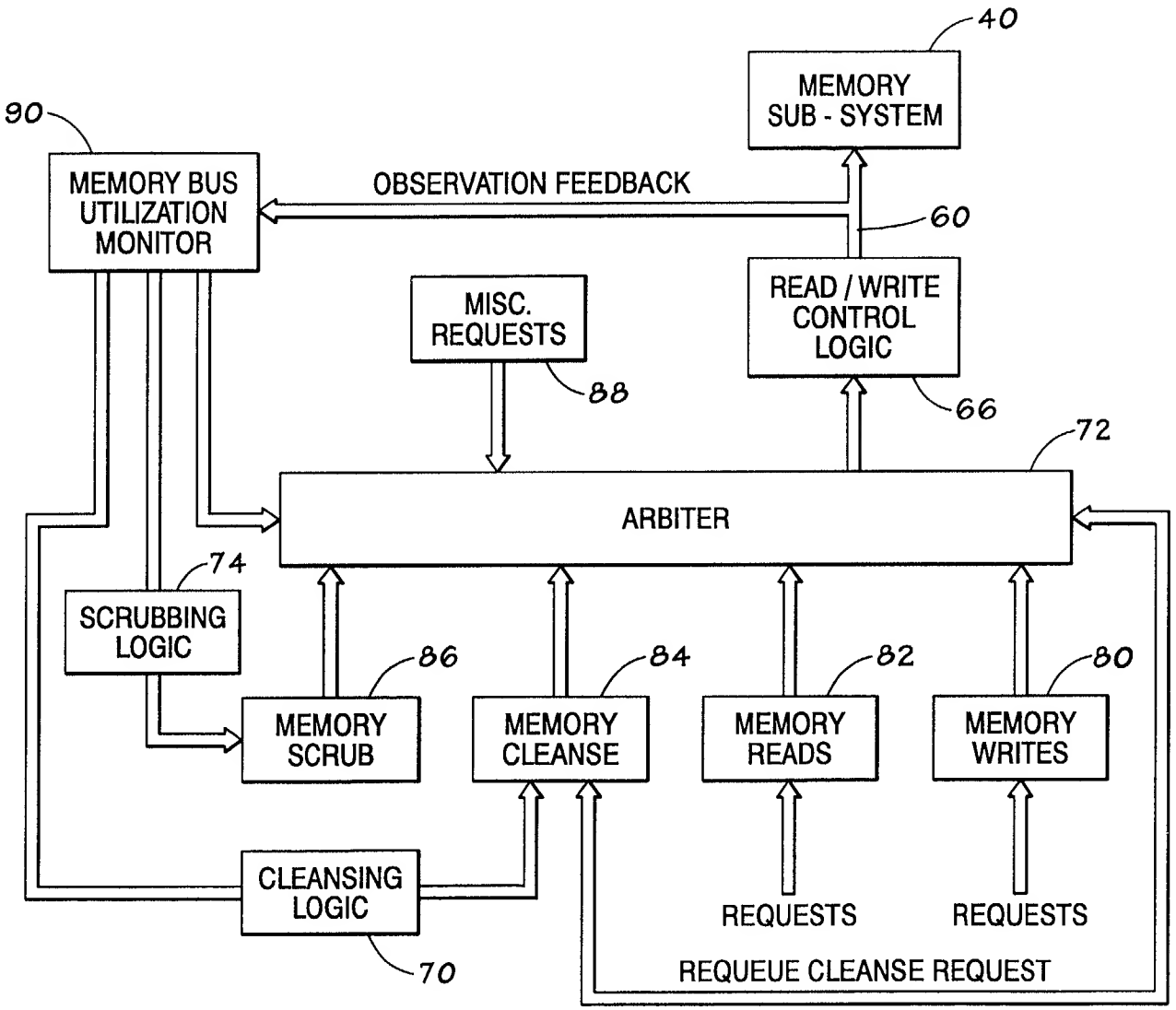



FIG. 7